What is claimed:

1. A semiconductor device comprising a memory region, first, second and third transistor regions including field effect transistors that operate at different voltage levels,

the memory region including a split-gate non-volatile memory transistor,

the first transistor region including a first voltage-type transistor that operates at a first voltage level,

the second transistor region including a second voltage-type transistor that operates at a second voltage level, and

the third transistor region including a third voltage-type transistor that operates at a third voltage level,

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers, and includes gate insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

2. A semiconductor device according to claim 1, wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, and includes an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

3. A semiconductor device according to claim 2, wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein

the intermediate insulation layer is formed from at least three insulation layers, wherein first and second outermost layers of the three insulation layers respectively contact the floating gate and the control gate and are composed of insulation layers that are formed by a thermal oxidation method.

4. A semiconductor device according to claim 3, wherein the second outermost layer that contacts the control gate is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

5. A semiconductor device according to claim 3 , wherein the intermediate insulation layer includes an insulation layer between the first and the second outermost layers, that is formed by a CVD method.

6. A semiconductor device according to claim 5, the third voltage-type transistor has a gate insulation layer formed in the same step in which the intermediate insulation layer of the non-volatile memory transistor is formed, the gate insulation layer of the third voltage-type transistor being formed from at least three insulation layers.

7. A semiconductor device according to claim 6, wherein the first voltage-type transistor has a gate insulation layer having a thickness of 3 – 13 nm.

8. A semiconductor device according to claim 7, wherein the second voltage-type transistor has a gate insulation layer having a thickness of 4 – 15 nm.

9. A semiconductor device according to claim 8, wherein the third voltage-type transistor has a gate insulation layer having a thickness of 16 – 45 nm.

10. A semiconductor device according to claim 9, wherein the non-volatile memory transistor has an intermediate insulation layer having a thickness of 16 – 45 nm.

11. A semiconductor device according to claim 3, wherein the first outermost layer has a thickness of 5 – 15 nm, and the second outermost layer has a thickness of 1 – 10 nm.

12. A semiconductor device according to claim 1, wherein the first voltage level that operates the first voltage-type transistor is 1.8 – 3.3 V, the second voltage level that operates the second voltage-type transistor is 2.5 – 5 V, and the third voltage level that operates the third voltage-type transistor is 10 – 15 V.

13. A semiconductor device according to claim 12, further comprising at least one flash-memory.

14. A semiconductor device according to claim 13, further comprising another circuit region mounted together.

15. A semiconductor device according to claim 14, wherein the another circuit region includes at least a logic circuit.

16. A semiconductor device according to claim 15, wherein the first voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder, an address buffer and a control circuit.

17. A semiconductor device according to claim 15, wherein the second voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder and an interface circuit.

18. A semiconductor device according to claim 15, wherein the third voltage-type transistor is included in at least one circuit selected from a group consisting of a voltage generation circuit, an erase voltage generation circuit and a step-up voltage circuit.

19. A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers.

20. A semiconductor device according to claim 19, wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers.

21. A semiconductor device according to claim 19, wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein

the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate.

22. A semiconductor device as in claim 19, wherein the first voltage level is in the range of 1.8 to 3.3 V, the second voltage level is in the range of 2.5 to 5 V, and the third voltage level is in the range of 10 to 15 V.

23. A embedded semiconductor device comprising:

a plurality of semiconductor devices selected from the group consisting of a flash-memory, an SRAM memory, a RISC, an analog circuit, and an interface circuit;

the plurality of semiconductor devices being embedded in a sea of gates structure;

wherein at least one of the semiconductor devices comprises the structure of claim 19.

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